FORM PTO-1083				Ca. D	ocket	No	PD-8811
In re application Serial no.	Michio Asahina 07/780,455		•	Date:_	March	31, 19	993
Filed: 1393	October 22, 1991		93 A2R	- 1.1.T		_	
For:	SEMICONDUCTOR DEVI	ICE				Ö (ŀ
COMMISSIONER OF PATENTS	AND TRADEMARKS		2.1	J.J.,* }	h.C		APR 6 6
Washington, D.C. 20231						(.	
Sir:						***.	· ••• /
Transmitted herewith is	an amendment/respo	onse in the	above-	ldentif	ied a	pplicat	ion.
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Respectfully submitted,

M. Finkelstein, 21,082

SPENSLEY HORN JUBAS & LUBITZ ATTORNEYS AT LAW 1880 CENTURY PARK EAST, FIFTH FLOOR LOS ANGELES, CALIFORNIA 90067 (310) 553-5050

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PATENT B PD-8811FWC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

MICHIO ASAHINA

Serial No.: 07/780,455

Filing Date: October 22, 1991

For: SEMICONDUCTOR DEVICE

ART GROUP UNIT: 2

2508

APR 0 8 1993

EXAMINER:

S. Loke

AMENDMENT UNDER 37 C.F.R. § 1.116

Honorable Commissioner of Patents & Trademarks Washington, D.C. 20231

Dear Sir:

In response to the Examiner's Action dated January 4, 1993, kindly amend the above-identified application as follows:

IN THE CLAIMS:

Kindly cancel claim 26 and amend claim 25 as follows:

28. (AMENDED) A method of fabricating a semiconductor

device, comprising the steps of:

providing a substrate having a doped semiconductor region, the metal and a gate wiring, forming a lower conductor structure, and forming an insulating layer overlying said lower structure, and having at plates layer least one through opening extending to said lower conductor structure; and

forming an upper conductor structure on the insulating layer and causing the upper conductor structure to be connected to the lower conductor structure via the through opening;

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